CLAIMS

What is claimed is:

1. A programmable logic device, comprising:

a configurable logic block, the configurable logic block having function generators, each of the function generators configurable for at least two programmable mode functions;

the function generators coupled to an array of memory cells, the array of memory cells for storing configuration bits for configuring the function generators;

a primary address line coupled to each memory cell of the array of memory cells in a segment spanning two or more of the function generators;

a secondary address line coupled to groups of memory cells of the array of memory cells in separate segments, each of the separate segments spanning only one function generator of the function generators, the groups of memory cells being respectively associated with the function generators; and

a mask circuit configured to selectively communicate a signal of the primary address line to a segment of the secondary address line or to a ground responsive in part to the programmable mode function programmed.

2. The programmable logic device, according to claim 1, wherein the mask circuit is configured to selectively communicate the signal in partial response to operation state of the configurable logic block.

3. The programmable logic device, according to claim 2, wherein the operation state is a read state.

4. The programmable logic device, according to claim 2, wherein the operation state is a write state.

5. The programmable logic device, according to claim 2, wherein the at least two programmable mode functions are a lookup table and a random access memory.

6. The programmable logic device, according to claim 2, wherein the at least two programmable mode functions are a lookup table and a shift register.

7. The programmable logic device, according to claim 1, wherein the groups of memory cells are sub-arrays of the array of memory cells.

8. The programmable logic device, according to claim 7, wherein the sub-arrays have a row width of sixteen.

9. The programmable logic device, according to claim 7, wherein the sub-arrays have a column width of one.

10. The programmable logic device, according to claim 1, wherein a portion of memory cells of the array of memory cells is not part of the groups of memory cells respectively associated with the function generators.

11. The programmable logic device, according to claim 10, wherein each of the memory cells in the portion of memory cells is spaced apart for segmentation of the secondary address line.

12. The programmable logic device, according to claim 11, wherein each of the memory cells in the portion of memory cells is not usable.

13. The programmable logic device, according to claim 11, wherein the array of memory cells is eighty rows by one column.

14. The programmable logic device, according to claim 13, wherein the portion of memory cells are located at positions <16>, <22>, <39>, <56>, <62> and <79> of the array of memory cells.

15. A method for error checking, comprising:

configuring a programmable logic device, the programmable logic device having function generators and associated memory cells, the memory cells for storing data to configure the function generators;

providing a masking signal responsive to a write operation being active;

grounding address lines of a portion of the memory cells in partial response to the masking signal, the portion of the memory cells used for configuring a portion of the function generators as random access memories; and

allowing error checking of configuration bits in another portion of the memory cells while the write operation is active, the other portion of the memory cells used for configuring another portion of the function generators as lookup tables.

16. The method, according to claim 15, further comprising repeatedly checking for write operations for closed-loop error checking.

17. A method for error checking, comprising:

configuring a programmable logic device, the programmable logic device having function generators and associated memory cells, the memory cells for storing data to configure the function generators;

providing a masking signal responsive to a write operation being active;

grounding address lines of a portion of the memory cells in partial response to the masking signal, the portion of the memory cells used for configuring a portion of the function

generators as shift registers; and

allowing error checking of configuration bits in another portion of the memory cells while the write operation is active, the other portion of the memory cells used for configuring another portion of the function generators as lookup tables.

18. The method, according to claim 17, further comprising repeatedly checking for write operations for closed-loop error checking.

19. An apparatus for error checking, comprising:

means for configuring a programmable logic device, the programmable logic device having function generators and associated memory cells, the memory cells for storing data to configure the function generators;

means for providing a masking signal responsive to a write operation being active;

means for grounding address lines of a portion of the memory cells responsive to the masking signal, the portion of the memory cells used for configuring a function generator of the function generators as a random access memory; and

allowing error checking of configuration bits in another portion of the memory cells while the write operation is active, the other portion of the memory cells used for configuring another function generator of the function generators as a lookup table.

20. An apparatus for error checking, comprising:

means for configuring a programmable logic device, the programmable logic device having function generators and associated memory cells, the memory cells for storing data to configure the function generators;

means for providing an indicator as to whether a write operation is active;

means for grounding address lines of a portion of the

memory cells responsive to the write operation being active, the portion of the memory cells used for configuring a function generator of the function generators as a shift register; and

means for allowing error checking of configuration bits in another portion of the memory cells while the write operation is active, the other portion of the memory cells used for configuring another function generator of the function generators as a lookup table.

21. A method for read back of data, comprising:

configuring a programmable logic device, the programmable logic device having function generators and associated memory cells, the memory cells for storing data to configure the function generators;

providing a masking signal;

reading the memory cells to obtain data; and

masking a portion of the data responsive to the masking signal, the portion of the data masked associated with a portion of the memory cells, the portion of the memory cells used for configuring a portion of the function generators, the portion of the function generators configured for a type of component.

22. The method, according to claim 21, wherein the type of component is a random access memory.

23. The method, according to claim 21, wherein the type of component is a shift register.

24. A method for error checking, comprising:

configuring a programmable logic device, the programmable logic device having function generators and associated memory cells, the memory cells for storing data to configure the function generators;

static and continuous masking of a portion of the memory

cells used to configure a portion of the function generators as shift registers; and

allowing error checking of configuration bits in another portion of the memory cells while the write operation is active, the other portion of the memory cells used for configuring another portion of the function generators as lookup tables.

25. The method, according to claim 24, wherein the static and continuous masking comprises grounding address lines of the portion of the memory cells in partial response to a masking signal.

26. A method for error checking, comprising:

configuring a programmable logic device, the programmable logic device having function generators and associated memory cells, the memory cells for storing data to configure the function generators;

static and continuous masking of a portion of the memory cells used to configure a portion of the function generators as random access memories; and

allowing error checking of configuration bits in another portion of the memory cells while the write operation is active, the other portion of the memory cells used for configuring another portion of the function generators as lookup tables.

27. The method, according to claim 25, wherein the static and continuous masking comprises grounding address lines of the portion of the memory cells in partial response to a masking signal.